AMENDMENTS TO THE CLAIMS:

Claim listing:

1.– 219. (Canceled)

220. (New) A line decoder for a memory cell comprising:

a first input;

a second input;

an output; and

a circuit arranged to isolate the first and second inputs from the output comprising

a node switched to a first logic state when the output is switched to a second logic state,

a first transistor coupled to the first and second inputs and the node, the first transistor being switched off when the node is switched to the first logic state, thereby isolating the first and second inputs from the output, and

a second transistor coupled to the first transistor, the first input and the node, the second transistor coupling the first input to the node when the node is switched to the first logic state.

221. (New) The decoder of claim 220 wherein the second transistor comprises a gate and further comprising one or more inverters coupling the node to the gate.

222. (New) The decoder of claim 220 wherein the output is coupled to the node through an inverter.

223. (New) The decoder of claim 220 wherein the node is switched to the second logic state when the first input is switched to the second logic state and the first transistor is switched on when the node is switched to the second logic state.